REMARKS

In the Office Action of May 19, 2005, claims 5-15, 19-21 and 24 were indicated to be allowable if rewritten in independent form. Claims 1-4, 16-18, 22, 23 and 25 were rejected under 35 U.S.C. 103(a) as unpatentable over Thompson (U.S. Patent No. 6,873,211) in view of Lien (U.S. Patent Nos. 5,470,766 and 5,652,456).

Applicants' invention is a monolithically integrated amplifier comprising a heterojunction bipolar transistor (HBT) and a field effect transistor (FET) configured to current-limit a current to the HBT. As pointed out by applicants, such an amplifier has both a linear operating range and a saturated operating range. A power amplifier that operates in both ranges is particularly useful in wireless telephone communications because it can support multi-mode wireless applications. When the amplifier is also monolithically integrated as in applicant's invention, the amplifier can be fabricated in a very small space, making it even more attractive.

The '211 patent, which is the primary reference on which the claims have been rejected, describes in Fig. 3 a multimode bias circuit for a power amplifier 314. The circuit includes a linear mode bias circuit comprising current source 354, bipolar transistor 364 and FET 362 and a saturated mode bias circuit comprising a control voltage 356 and a resistor 358. The base of bipolar transistor 364 and the source of FET 362 are connected at node 368 which provides the DC bias for power amplifier 314. An RF input signal 370 is coupled to the base of power amplifier 314 by a capacitor 330.

A mode control signal 352 opens switch 360 and enables current source 354 to operate the amplifier in the linear mode and closes switch 360 and disables current source 354 to operate the amplifier in the saturated mode. In the linear mode, the circuit of Fig. 3 operates in similar fashion to the prior art circuit of Fig. 1 of the '211 patent. Current source 354 provides a

constant current into the collector of transistor 364 which causes transistor 364 to have a base-emitter voltage. Since the base of transistor 364 is coupled to the base of transistor 314, this base-emitter voltage of transistor 364 is also developed across transistor 314. Base current is supplied to the transistors 364 and 314 from supply voltage 320 via FET 362. Thus, in the linear mode a constant DC bias is generated at the base of transistor 314. As a result, the power output of the power amplifier is proportional to the input power provided by the RF signal 370 via capacitor 330.

In the saturated mode, the circuit of Fig. 3 operates in similar fashion to the prior art circuit of Fig. 2. The output power of the power amplifier is proportional to the amount of DC bias provided at the base of transistor 314 by control voltage 356. The control voltage 356 is applied to the collector of transistor 364 and the gate of FET 362. As the control voltage increases, the collector current in transistor 364 increases which increases the base voltage of transistor 364. Since the base of transistor 314 is coupled to the base of transistor 364, this also increases the base voltage of transistor 314. FET 362 functions as a voltage follower and allows base current to flow from supply voltage 320 to the base of transistor 314.

Of critical interest to the present discussion, the current in transistor 314 is not current limited by FET 362. Rather, in linear mode the current in transistor 314 is set by the current of current source 354 and in saturated mode it is set by the control voltage 356. Since, the '211 patent does not disclose an amplifier in which a FET is configured to current-limit a current to the HBT, claim 1 is patentable over this reference.

Dependent claims 2-4 and 16 are patentable for the same reason claim 1 is patentable. Dependent claim 2 is patentable for the additional reason that the FET of the '211 patent does

not current limit a base current. Dependent claim 3 is patentable for the additional reason that FET 362 of the '211 patent is gated while claim 3 requires that the FET be ungated.

Dependent claims 5-15 have been indicated to be patentable.

Independent claim 17 is patentable for the same reason claim 1 is patentable. Dependent claim 18 is patentable for the same reason claim 17 is patentable and for the additional reason claim 2 is patentable.

Dependent claims 19-21 have been indicated to be patentable.

Independent method claims 22 and 25 are patentable because they both recite the step of providing a monolithically integrated FET to limit the current flowing through an HBT. As emphasized in the discussion of claim 1, the '211 patent does not disclose the use of an FET to limit the current flowing through an HBT.

Dependent claim 23 is patentable for the same reason claim 22 is patentable. In addition, claim 23 is patentable because it specifies that the FET reduces a variation of output power to a change in load phase. There is no disclosure of this in the '211 patent.

Dependent claim 24 has been indicated to be patentable.

No additional fee is believed to be due. If, however, a fee is due, please charge such fee to Morgan, Lewis & Bockius LLP Deposit Account No. 50-0310.

If the Examiner believes a telephone interview would expedite prosecution of this application, he is invited to call applicant's attorney at the number given below.

Respectfully submitted,

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